



MULTIPLEXED ARCHITECTURE

This multiplexed architecture 16x64 provides an efficient and cost-effective solution to Original Equipment Manufacturers for integration into third-party systems. The board and dynamic-link libraries (dlls) are available.

GENERAL

L x W x H: 210mm x 100mm x 50mm Weight: ~500 g

HARDWARE CONFIGURATION

Multiplexed architecture: 16x64

LIBRARIES

dll provided

EMBEDDED PROCESSORS

FPGA on CPU-board

PULSERS

Adjustable voltage: 20 to 80V with 1V step

Rise time < 10 ns (80V, 50 Ω)

Negative rectangular pulse, adjustable width: 30 ns to 625 ns, step of 2.5 ns

Max. PRF: 30 KHz

RECEIVERS

Bandwidth: 0.8 to 20MHz

Adjustable analog DAC on 80 dB (max. 40 dB/μs) synchronized on events

Adjustable gain on each channel from 0 to 80 dB

Cross-talk between two channels > 50 dB, max. input signal amplitude: 0.8 Vpp

DIGITIZER

Max. sampling frequency: 100 MHz - Adjustable from 100 MHz to 6.6 MHz

Global delay: 0 up to 1.6 ms, step of 10 ns

Range : 10 bits

Delay-laws at transmission/reception: 0 to 20 μs, step of 2.5 ns

Input impedance: 50 Ω | FIR filters

Digitizing depth: up to 50,000 samples (8,000 samples max. per elementary channel)

I/O

1 Hypertronix connectors

1 USB2, 2 LEMO connectors (type 00)

3 encoders input, 1 external trigger

External power supply input